

## WHAT IS CLAIMED IS:

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1. A system semiconductor device, comprising:  
 a system LSI cell portion which includes a plurality of functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and  
 a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other.
  2. A system semiconductor device as claimed in claim 1, wherein:  
 a plurality of the system LSI cell portions are formed on a semiconductor wafer,  
 a plurality of the global wiring layers are formed on the semiconductor substrate, and  
 the semiconductor wafer and the semiconductor substrate are laminated, diced and separated to obtain a plurality of the system semiconductor devices.
  3. A system semiconductor device claimed in claim 1, wherein:  
 the global wiring layer comprises;  
 a first wiring layer formed on the semiconductor substrate,  
 an insulating layer formed on the first wiring layer, and  
 a second wiring layer and an adhesive layer formed on the insulating layer.
  4. A system semiconductor device claimed in claim 1, wherein:  
 the global wiring layer comprises;  
 a first wiring layer formed on an organic substrate,  
 an insulating layer formed on the first wiring layer, and  
 a second wiring layer and an adhesive layer formed on the insulating layer.

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5. A system semiconductor device as claimed in claim 1, wherein:  
 the global wiring layer comprises;  
 a first wiring layer formed on the semiconductor substrate,  
 an insulating layer formed on the first wiring layer,  
 a second wiring layer formed on the insulating layer, and  
 inner bumps formed on the second wiring layer.

6. A system semiconductor device claimed in claim 1, wherein:  
 the global wiring layer comprises;  
 a first wiring layer formed on an organic substrate,  
 an insulating layer formed on the first wiring layer,  
 a second wiring layer formed on the insulating layer, and  
 inner bumps formed on the second wiring layer.

7. A system semiconductor device as claimed in claim 3, wherein;  
 the insulating layer includes a via which electrically connects the  
 first wiring layer with the second wiring layer.

8. A system semiconductor device as claimed in claim 1, wherein:  
 the global wiring layer has bumps for electrically connecting to an  
 external circuit on a surface thereof.

4. 9. A system semiconductor device as claimed in claim 1, wherein:  
 the global wiring layer includes buried vias which electrically  
 connect the functional blocks to an external circuit.

5. 10. A system semiconductor device as claimed in claim 1,  
 wherein:

the global wiring layer has at least one or more of the wiring layers.

11. A system semiconductor device as claimed in claim 3,  
 wherein:

the global wiring layer has at least one or more of the insulating  
 layers.

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12. A method of manufacturing comprising the steps of:

- fabricating a system LSI cell portions on a semiconductor chip,
- fabricating a global wiring layer on a semiconductor substrate, and
- laminating the system LSI cell portions on the global wiring layer so that the functional blocks are electrically connected to the global wiring layer.

fabricating a global wiring layer  
conductor substrate, and  
laminating the system LSI cell p  
that the functional blocks are elect

laminating the system LSI cell p  
that the functional blocks are elect

~~10-13.~~ A method as claimed in claim 12,

forming a plurality of the system conductor wafer.

forming a plurality of the global  
rate.

laminating the semiconductor wafer, and

dicing and separating the laminated conductor substrate to obtain a plurality of pieces.

11. ~~14~~. A method as claimed in claim 12 <sup>9</sup>

the global wiring layer is formed by depositing, on an insulating layer, a second wiring layer on a semiconductor substrate.

semiconductor substrate.

~~14.15~~ 9. A method as claimed in claim 12,

the global wiring layer is formed by a first wiring layer, an insulating layer, a second wiring layer, and a second insulating layer, all of which are formed on an organic substrate.

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is formed

wiring layer, a second wiring layer, an insulating layer, and inner bumps on the semiconductor substrate.

17. A method as claimed in claim 12, wherein:

the global wiring layer is formed by sequentially laminating a first wiring layer, an insulating layer, a second wiring layer, and inner bumps on an organic substrate.

~~12. 18.~~ A method as claimed in claim ~~14~~<sup>11</sup>, further comprising the following step:

forming a via for electrically connecting the first wiring layer with the second wiring layer in the insulating film.

~~15. 19.~~ A method as claimed in claim ~~12~~<sup>9</sup>, further comprising the following step:

forming bumps for electrically connecting to an external circuit on the global wiring layer.

~~16. 20.~~ A method as claimed in claim ~~12~~<sup>9</sup>, further comprising the following step:

forming buried vias for electrically connecting the functional blocks to an external circuit in the global wiring layer.

~~17. 21.~~ A method as claimed in claim ~~12~~<sup>9</sup>, further comprising the following step:

forming at least one or more of the wiring layers in the global wiring layer.

~~13. 22.~~ A method as claimed in claim ~~14~~<sup>11</sup>, further comprising the following step:

forming at least one or more of the insulating layers in the global wiring layer.

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